Processor Board

Panther processor Board
The Panther processor board is based on the radiation hardened COLE ASIC developed by RUAG Space AB. COLE consists of a fault-tolerant SPARC® processor and all necessary I/O interface functions.
**Key characteristics**

**COLE processor function**
The processor is a SPARC® Version 8 processor, LEON-2 FT, especially designed for critical space applications. One of its main features is a very high degree of internal error detection. Most of the internal errors are directly detected and signalled to the outside world for proper handling.

A high-performance built-in IEEE-754 floating-point unit is included, that also includes support for concurrent error detection. The processor has 32 Kbytes instruction cache and 16 Kbytes data cache. A dedicated Debug Support Unit (DSU) is provided to be able to put the processor in debug mode, allowing access to all processor registers and cache memories. The DSU also contains a trace buffer which stores executed transfers on the COLE internal bus.

The processor board is available in a variant equipped with an AX2000 Field Programmable Gate Array (FPGA) intended for customer defined control and data interfaces. Alternatively, it can be used for customer designed hardware accelerated processing such as Fast Fourier Transform (FFT), GPS Receiver or data compression to give a few examples.

**Processing performance**
The board uses typically operates at a processor frequency of 64 or 80 MHz. At 80 MHz the performance is approximately 70 Dhrystone MIPS and maximum 22 MFLOPS.

**Memory subsystem**
The working memory for the processor consists of up to 8 Mbytes of Error Detection and Correction (EDAC) protected SRAM or 512 Mbytes SDRAM. Since the EDAC is included in the COLE ASIC this means that there are very few memory or interconnection errors that will not be detected. COLE includes a Memory Management Unit (MMU) to provide virtual memory and memory protection. Accesses to unimplemented memory areas are also detected and reported by the MMU.

The boot software is normally located in 32 or 64 Kbytes of PROM. The application software may be stored in up to 8 Mbytes of EEPROM. The design also provides a possibility to boot directly from the EEPROM or RAM, in which case the PROM devices are not mounted.

**Interfaces**
The following interfaces can be provided:

- Two dual-redundant MIL-STD-1553B buses with Bus Controller and Bus Monitor capabilities. One of the bus interfaces can also function as Remote Terminal.

- Two Controller Area Network (CAN) buses, which can be used in a redundant bus system.

- Up to eight SpaceWire (ECSS-E-50-12A) point-to-point links with LVDS interfaces, providing high-speed serial connections at up to 200 Mbps.

- Up to five Universal Asynchronous Receiver/Transmitter (UART) interfaces, which three high-speed with Direct Memory Access (DMA) support provided for typical control and data acquisition purposes.

- Packet Wire links (synchronous serial links with clock, data, strobe and ready) with a maximum data rate of 32 Mbps. There are up to two receiver links and up to two transmitter links.

- MIL-STD-1553B Bus Controller or OBDH Central Terminal with digital interfaces, available via the backplane connector.
• Twelve general-purpose inputs or outputs, which primarily are indented as interrupt or status inputs. Four of these can be configured as signals received via the backplane connector. It is also possible to configure two of the inputs as signals received via the external connector.

• Eight synchronization pulse outputs, programmable to various frequencies that are synchronized to the 1Hz On Board Time reference.

Test interfaces
Two of the RS-422 UART interfaces + one SpaceWire interface can be used for communication with a host computer during software development. The enhanced on-chip Debug Support Unit provides access to internal functions even while the processor is executing. The SpaceWire test I/F can be used to perform real-time dump of selected parameters or a compressed program flow. An additional LICE serial test interface can be used for program flow tracing.

Mechanical concept
The design is implemented on a multi-layered printed circuit board (PCB). To allow efficient mounting of components on both sides of the PCB half blind vias are used. The PCB is equipped with a frame for mechanical support and thermal conduction. The frame is adapted to fit the RUAG Space AB mechanical concept.

The external connectors are one HDD-78 pin connector for I/O communication, two HDD-15 pin for MIL-STD-1553B communication, one HDD-62 socket connector as test connector and the SpaceWire MDM-9 connectors. The internal backplane connectors are two 174-pin CSD connectors, mounted opposite to the external connectors.

Software Development Environment
The board is provided with a Boot Software as well as Hardware Driver Software for supported interfaces. The GNU cross compiler (GCC) suite can be used for development in C and C++ for the COLE target. Support for the RTEMS operating system is available in terms of a COLE Board Support Package. A host platform independent COLE specific development tool suite, COLE Tools, that utilises the enhanced Debug Support Unit is available.

The core of the COLE Tools is the COLE Broker, which allows multiple clients, connected via TCP/IP sockets, to share the same links (SpaceWire and UART:s) towards COLE. The main clients are:

• COLEmon: GDB remote target monitor proxy for source level debugging
• Console: COLE UART debugging I/O
• COLE Trace: Execution tracing control and logging
• Inspector COLE: Non-intrusive browsing and monitoring of internal COLE registers and memory, as well as modifying, e.g. for error injection

The COLE Broker uses an open XML based client protocol, allowing the user to implement application specific clients.

The free and open source Eclipse platform is supported. Eclipse provides an integrated development environment where the source code editor, configuration tool, compiler, debugger, and other development tools are all accessed through one graphical user interface. Eclipse support is available for compilers such as the GCC suite, configuration tools such as Subversion and ClearCase, and a multitude of other development tools. For COLE, Eclipse support is provided for UART I/O, and source level debugging with GDB using COLEmon.
The fundamentals of COLE, memory and interfaces are illustrated in the block diagram.

**Budgets**
- Processing performance: 70 Dhrystone MIPS and 22 MFLOPS
- Printed Circuit Board size: 257 x 185 mm
- Module size: 261 x 205 mm x 36 mm
- Power consumption: 6 W
- Reliability (QML-Q): 900 FITS
- Design life time: 15 years in Geostationary or Low Earth Orbit

**Power Supplies**
The Panther board requires 3.3V and 5V for MIL-STD-1553B or CAN transceiver devices, from the backplane connector.

RUAG Space AB is an international, independent supplier of space equipment. The company's main products are computers, microwave electronics and antennas for satellites and control and separation systems for launch vehicles. The company has its headquarters in Gothenburg, Sweden, and a division located in Linköping, Sweden. RUAG Space AB has approximately 380 employees.